THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 30

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte SHINZO SAKUMA, and SAMPEI MIYAMOTO

Appeal No. 97-4425
Application 08/619,418[1]

ON BRIEF

Before KRASS, FLEMING and LEE, Administrative Patent Judges.

LEE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 11-16, 18 and 19. Claims 1-10 have been canceled. Claim 20 has been allowed.

Reference Relied on by the Examiner

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[1] Application filed March 21, 1996. According to the appellants, it is a continuation of Application 08/420,335, filed April 11, 1995, now abandoned, which is a continuation of Application 08/243,585, filed May 16, 1994, now abandoned, which is a division of Application 07/986,998, filed December 7, 1992, now Patent No. 5,313,426.

Kohno et al. (Kohno) Patent No. 5,072,425 Dec. 10, 1991

Rejection on Appeal

Claims 11-16, 18 and 19 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kohno. Claim 17 has been objected to as being dependent from a rejected claim.

The Invention

The invention is directed to sense amplifier drive circuits in a semiconductor memory. The sense line and a conductor element are connected to both a first node of a first sense amplifier and the second node of a second sense amplifier. Both the sense line and the conductor element are for transferring control signals to the sense amplifiers. Representative independent claims 11 and 19 are reproduced below.

11. A semiconductor memory device having a semiconductor substrate having a major surface thereof, comprising:

a first pair of bit lines, formed over the major surface, having first and second bit lines, said first pair of bit lines being coupled to a first memory cell, said first memory cell causing a first potential difference between said first and second bit lines;

a second pair of bit lines, formed over the major surface, having third and fourth bit lines, said second pair of bit lines being coupled to a second memory cell, said second memory cell causing a second potential difference between said third and fourth bit lines;

a first sense amplifier having a first node, said first sense amplifier being connected to the first pair of bit lines, for amplifying the first potential difference between said first

and second bit lines in response to a first sense amplifier control signal during a sensing operation;

a second sense amplifier having a second node, said second sense amplifier being connected to the second pair of bit lines, for amplifying the second potential difference between said third and fourth bit lines in response to the first sense amplifier control signal during the sensing operation;

a first sense line connected to said first and second nodes for transferring the first sense amplifier control signal to said first and second sense amplifiers, said first sense line being formed over the major surface; and

a first conductive element connected to said first and second nodes and formed in the major surface, for transferring the first sense amplifier control signal to both said first and second sense amplifiers during the sensing operation.

19. A semiconductor memory device having a semiconductor substrate having a major surface thereof, comprising:

a first pair of bit lines;

a second pair of bit lines;

a first sense amplifier having a first node, said first sense amplifier being connected to the first pair of bit lines, for amplifying a potential difference between said first pair of bit lines in response to a sense amplifier control signal during a sensing operation;

a second sense amplifier having a second node, said second sense amplifier being connected to the second pair of bit lines, for amplifying a potential difference between said second pair of bit lines in response to the sense amplifier control signal during the sensing operation;

a sense line connected to said first and second nodes for transferring the sense amplifier control signal to said first and second sense amplifiers, said sense line being formed over the major surface; and

a conductive element connected to the first and second nodes for transferring the sense amplifier control signal to both said first and second sense amplifiers during the sensing operation.

Opinion

Our opinion is based solely on the arguments made by the appellants in their briefs. Arguments which could have been but in fact are not made by the appellants are considered to be waived and will not be considered or addressed.

Anticipation is established only when a single prior art reference discloses, either expressly or under the principles of inherency, each and every element of the claimed invention. In re Spada, 911 F.2d 705, 708, 15 USPQ2d 1655, 1657 (Fed. Cir. 1990); RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984).

The issue in this case centers about whether Kohno discloses "a first conductive element" as is recited in independent claim 11. According to claim 11, the first conductive element is connected to the first and second nodes and is formed in the "major surface" of the substrate. The function of the first conductive element is to transfer control signals to the first and second amplifiers during the sensing operation. The

appellants assert (Reply at 3, lines 14-15) that in case there is some delay along the sense line, control signals can still be provided along the conductive element without incurring a delay.

On page 10 of the answer, the examiner identifies what he considers to be the conductive element in Kohno, i.e., conductive line element L32. However, as is discussed by Kohno in column 13, lines 49-60, conductive element L32 is formed in a second wiring layer formed above the memory cell. Thus, the appellants are correct that L32 is not formed on the major surface of the substrate.

On page 11 of the answer, the examiner inexplicably switched what he regards as the conductive element. Here, he regards the unnamed connection between line L1 and the sense amplifier as the conductive element. It is inappropriate to switch in mid-stream without re-establishing all that is required of the conductive element as claimed, e.g., connection to the first and second nodes. What is true for L32 is not automatically true for the unnamed segment connecting L1 to the sense amplifier. As is shown in Kohno's Figure 11, L32 and the unnamed element are clearly different elements.

The appellants are correct that there is no basis for the examiner to assume that the unnamed element connecting the line

L1 to the sense amplifier is formed "in the major surface" of the semiconductor substrate. The examiner made no explanation as to why it necessarily must be so. There is nothing to indicate that this claimed feature is an inherent characteristic of Kohno. The examiner has not articulated sufficient basis or pointed to sufficient evidence to find that the unnamed conductive element is formed "in the major surface" of the substrate. Note also that from Figure 11 of Kohno, it does not appear that the unnamed element extends in the same plane of the major surface of the substrate. Accordingly, Kohno has not been shown to anticipate claim 11 or the claims depending therefrom. A finding of anticipation cannot be based on mere speculation or conjecture.

For the foregoing reasons, the rejection of claim 11 and claims depending either directly or indirectly from claim 11 cannot be sustained.

Claim 19, on the other hand, does not require that the conductive element be formed on the major surface of the semiconductor substrate. Thus, the argument about the conductive element being formed on the major surface of the semiconductor substrate does not apply to claim 19.

With respect to independent claim 19, the appellants argue that the claimed invention allows the sense amplifier control

signals to be provided through both the sense line and the conductive element such that if there is a delay along the sense line at any contact point, those signals can still be provided along the conductive element without a delay (Br. at 18, 19, 20; Reply at 3). The appellants point out (Reply at 3, lines 8-15) that this functionality and advantage is provided by having the diffusion line (conductive element) connected directly to the sense amplifiers and the sense line directly connected to a number of metal diffusion contacts which are, in turn, connected to the diffusion line or the conductive element. For instance, in the brief on page 20, lines 4-10, the appellants state:

> In Kohno et al., L32 [conductive element] is connected to L1 which is directly connected to the sense amp. In contrast, in the present invention, the sense line SLN is connected to the sense amplifiers 140-1, for example, by contacts C4 and C5 to line D2 [conductive element], and to sense amplifier 140-2 by contacts C5 and C6 to D2 [conductive element]. Hence, in the present invention, there are multiple contacts for the sense line to connect to the sense nodes of both the first amplifier and second amplifier. This prevents the delays possible in Kohno et al. This cannot be done with Kohno et al.

The argument, however, is not commensurate in scope with what is claimed. First, the function or capability of providing control signals through the conductive element without delay when there is a delay along the sense line is not recited in claim 19. Secondly, claim 19 does not require directly connecting the

conductive element to the sense amplifiers. The language of the claim is sufficiently broad to cover directly connecting the sense line to the sense amplifiers and indirectly connecting the conductive element to the sense amplifiers through the sense line. The claim requires only that both the sense line and the conductive element be connected to the first and second nodes.

The appellants argue (Reply at 2, lines 18-19) that the examiner has provided no explanation as to how the conductive element is connected to the first and second nodes. However, the examiner clearly indicated that the first node is the node at the intersection of L1 and L32 and that the second node is also the node at the intersection of L1 and L32 (answer at 5, lines 7-8 and lines 13-14). Figure 8B of Kohno clearly illustrates that the conductive line element L32 is connected to that common node.

The appellants have not argued that the first and second nodes cannot be a common node. In any event, in light of this specification, we agree with the examiner that the claim can reasonably be interpreted such that the first and second nodes can be a common node. Note first and second nodes S1 and S3 in Figure 1 of the appellants' specification, which are essentially the same node by being directly connected to each other.

For the foregoing reasons, we sustain the rejection of claim

19.

Conclusion

The rejection of claims 11-16 and 18 under 35 U.S.C. § 102(b) as being anticipated by Kohno is reversed.

The rejection of claim 19 under 35 U.S.C. § 102(b) as being anticipated by Kohno is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

ERROL A. KRASS Administrative Patent Judge	)
MICHAEL R. FLEMING Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
JAMESON LEE Administrative Patent Judge	)

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